G.711 PCM Codec

Data Sheet

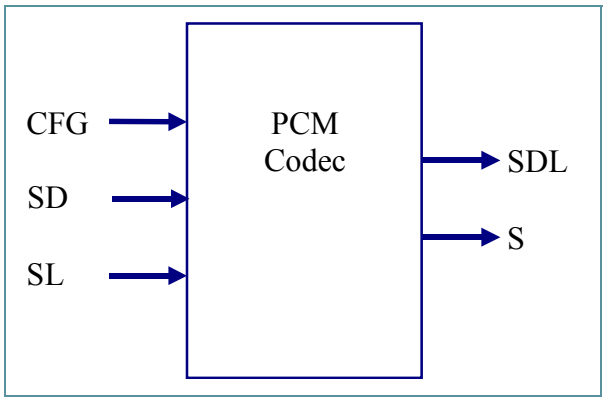
AMPHION

Executive Summary

Module	G.711 - PCM
Device	QuickDSP QL7180
Speed Grade	-7 (Worst Case)
Unbuffered Logic Cell Utilization	73 / 4,032
Buffered Logic Cell Utilization	119 / 4,032
ECU Utilization	3 / 18
Maximal Clock Frequency	39 MHz

Device Highlights

- PCM - Pulse Code Modulation
- CCITT - International Telegraph and Telephone Consultative Committee
- Verilog - Hardware description language
- Transcoding- The process of converting a speech signal to and from PCM and uniform PCM format.



General Description

Speech signals can have a large dynamic range in the region of 60 dBs, therefore requiring a large number of quantization levels. However, the accuracy of the lower amplitude parts of the signal is more important than the larger amplitude parts, hence a non-linear method of quantization can be used to reduce the data rate. The idea here is to vary the distance between quantization reconstruction levels so that the distance increases as the amplitude of sample increases. To do this, the sampled signal is first passed through a logarithmic compressor and then uniformly quantized. In reverse the signal is passed through an expander with the inverse transform characteristics of the compressor. This process is referred to as companding. Two particular logarithmic quantization techniques for PCM, as defined by CCITT are in worldwide use. These are, the American μ–law PCM and the European A–law PCM, as defined below:

A-Law:

$$c(x) = \begin{cases} \dfrac{A|x|}{1+\log_e A}\operatorname{sgn}(x) & 0 \le \dfrac{|x|}{x_{\max}} \le \dfrac{1}{A} \\ x_{\max}\dfrac{1+\log_e(A|x|/x_{\max})}{1+\log_e A} & \dfrac{1}{A} \le \dfrac{|x|}{x_{\max}} \le 1 \end{cases}$$

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last updated 5/25/01

μ-Law:

$$c(x) = x_{\max} \frac{\log_e(1+\mu|x|/x_{\max})}{\log_e(1+\mu)} \operatorname{sgn}(x)$$

The G-711 standard is the most common compression algorithm for worldwide telecommunication networks, and is found on T1, E1 and ISDN lines. Basically, the G-711 standard compresses a 13-bit A-law or 14-bit μ–law linear PCM sample to an 8 bit logarithmic representation. Figure 1 shows the logarithmic partitioning of the input values for encoding using A-law PCM. The diagram does not give the full detail of the scheme but depicts the basic idea behind the technique. The encoding of negative values is performed using a similar structure whereby the smaller the magnitude of the negative value, the smaller the segment number. The μ-law is similar and the conversion to and from it is incorporated within the standard.

Both techniques allow only 8-bits to be used per a sample with a resulting speech quality almost indistinguishable from the original signal at a significantly reduced data rate of 64 kbits/s. This resulting PCM signal provides a quality benchmark for all other telephone compression algorithms. At the receiving end the data is then converted back to the linear scale (13-bits for A-law and 14-bits for μ–law).

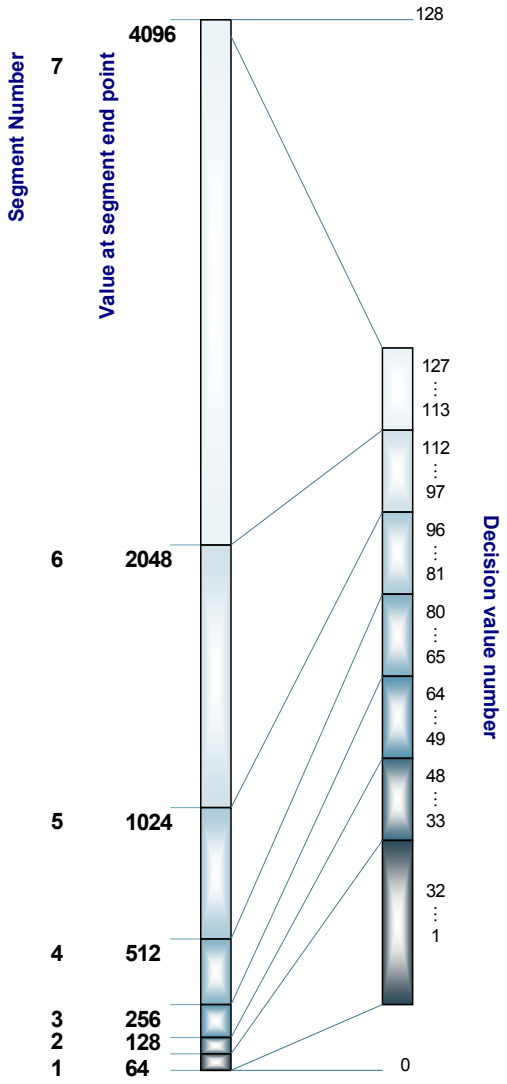


FIGURE 1: A-law encoding for positive input values

General Features

The ISS CSC4910AA PCM codec has the following features

- µ-Law or A-Law encode/decode operation.
- Even bit inversion option for A-Law, or all bit inversion option for µ-Law.
- Data format selection: Signed magnitude or Two's complement.
- Conforms fully to CCITT G.711 Standard

- Digital phone samples (PCM) must be decompressed (8 bits to 13/14 bits) before using more aggressive algorithms suitable for VoIP applications.
- Only then can ADPCM/CELP etc be applied before suitable framing, protocol etc can be used.
- The system operates in reverse with the CELP or ADPCM block decompressing the transmitted VoIP data which then should be PCM compressed (G711 Compressor) before transmission to a digital phone line user

Below is illustrates the use of G711 in a VoIP system.

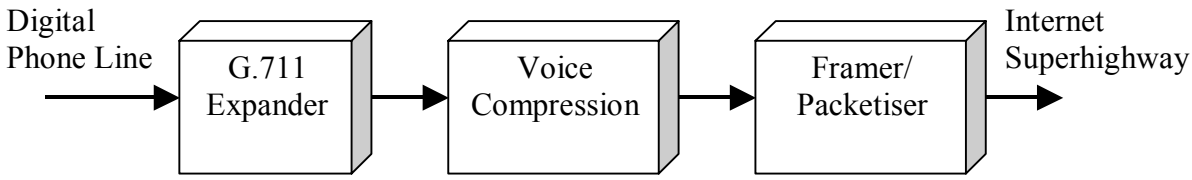
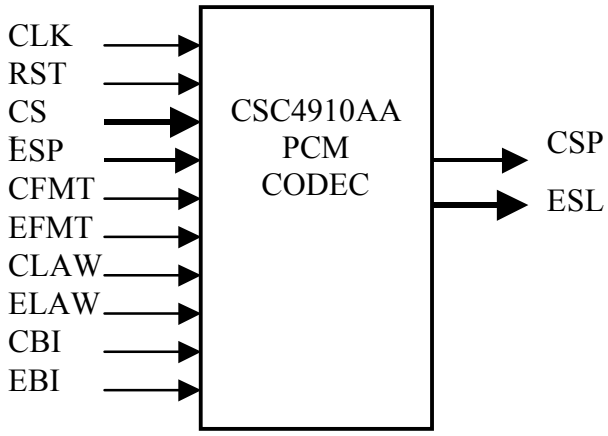


FIGURE 2: G.711 in a VoIP system

I/O Descriptions

Unless otherwise stated all signals are active high and bit(0) is the least significant bit.



Pin	I/O	Width (Bits)	Description
CLK	I	1	Clock input - rising edge active
RST	I	1	Global reset signal
CSL	I	14	Input uniform PCM word for encoding, using all 14 bits (μ-law) or 13 bits, S(13:1) (A-law).
ESP	I	8	m-Law/A-Law PCM input word for decoding.
CFMT	I	1	Compressor data format: 0: sign-magnitude, 1: two's complement.
EFMT	I	1	Expander data format: 0: sign-magnitude, 1: two's complement.
CLAW	I	1	Compressor Law selection: 0 = μ-Law, 1 = A-Law.
ELAW	I	1	Expander Law selection: 0 = μ-Law, 1 = A-Law.
CBI	I	1	Compressor bit inversion: 0 = no bits inverted, 1 = Even bits inverted (A-Law) or All bits inverted (m-Law)
EBI	I	1	Expander bit inversion: 0 = no bits inverted, 1 = Even bits inverted (A-Law) or All bits inverted (μ-Law)
ESL	O	14	Uniform PCM signal from decoding (14-bits μ-Law/13-bits A-law)
CSP	O	8	μ-Law/A-Law PCM encoded output word.

TABLE 1 : I/O Descriptions

Operation of the CSC9410AA

Law

The compression and expansion law can be specified using the CLAW and ELAW signals respectively. The assertion of one of these signals specifies A-Law for the corresponding coder otherwise μ-Law is used.

Bit Inversion

Often there will be a majority zeros in the compressor output. For this reason the Bit Inversion option is available, and controlled for the expander by the EBI signal, and for the compressor by the CBI signal. If enabled (asserted) for A-Law even bit inversion is performed, while for μ-Law all bit inversion is performed.

IO Interface

For m-Law all 14 bits IO bits are used, however for A-Law the upper 13 bits are used. This is illustrated in Figure 3 below.

Data Format

The encode/decode data format is specified via the two signals EFMT and CFMT. Upon assertion of CFMT the encode data format will be in two's complement, otherwise the format will be sign magnitude format, similarly the decode data format, is controlled by EFMT.

When the format is specified as sign-magnitude, the 14-bit data is represented as follows:

The MSB is the sign ('0': positive, '1': negative), and the remaining bits represent the magnitude. For m-law all of the remaining 13-bits represent the magnitude i.e.: second MSB to LSB [12:0], while for A-law the upper 12 of the remaining 13 bits represent the magnitude i.e.: second MSB to second LSB - [12:1]

When the format is specified as two's complement, the 14-bit data is represented as follows:

For m-Law all the bits represent the two's complement value, and for A-Law the upper 13 bits [13:1] represent the value.

13 bits [13:1] represent the value.

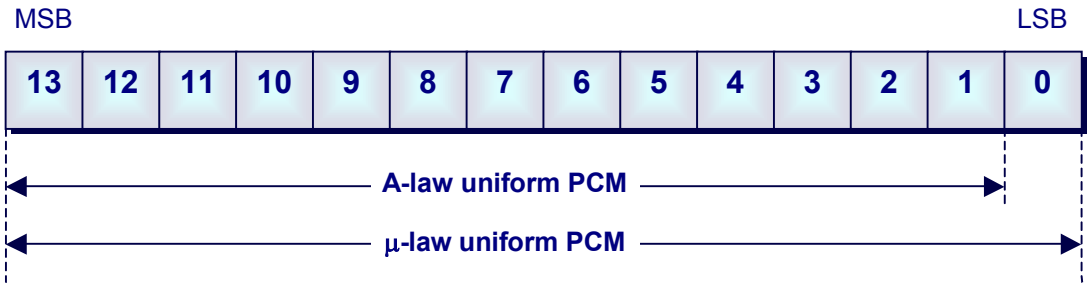


FIGURE 3: IO Data format

I/O Timing

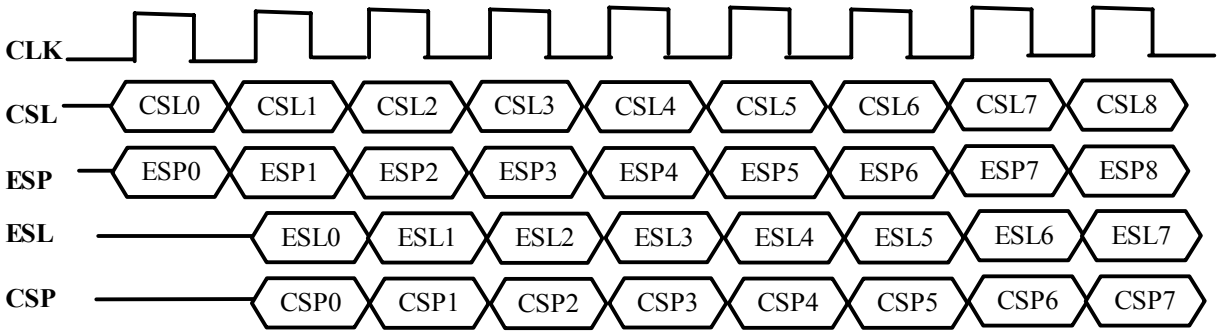


FIGURE 4: I/O Timing

All the IO's are registered so there is 2 clock-cycle transcoding delay for each coder.

CSL - Compressor Input

ESP - Expander Input

ESL - Expander Output

CSP - Compressor Output

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