LSI/CSI

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LS7290

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STEPPER MOTOR CONTROLLER

FEATURES:

- Controls Bipolar and Unipolar Motors
- Cost-effective replacement for **L297** in Bipolar applications
- Full, 1/2, 1/4, 1/8, 1/16, 1/32, step mode selected with 3 mode inputs
- Direction control
- Reset input
- Step control input
- Enable input
- PWM chopper circuit for current control
- 8-bit PWM resolution
- Two overcurrent sensor comparators with external reference input
- Step control frequency and duty cycle controlled by an external frequency source or by an internal crystal controlled oscillator (typically 8MHz)
- All inputs and outputs TTL/CMOS compatible (TTL for 5V operation)
- 3V to 5.5V Operation (V_{DD} - V_{SS}).
- LS7290 (DIP), LS7290-S (SOIC), LS7290-TS (TSSOP) **- See Figure 1 -**

DESCRIPTION:

The LS7290 generates Phase Drive outputs and PWM outputs for controlling two-phase Bipolar motors or four-phase Unipolar motors, respectively. The LS7290 contains a mode controlled look-up table for generating the motor duty cycle drive sequences. There are four outputs which are used to drive two H-Bridges for the two motor windings in the Bipolar motor or the four Driver Transistors for the two center-tapped windings in the Unipolar motor (Refer to Table 2). The LS7290 can step a motor in full steps, half steps or in 1/4, 1/8, 1/16 or 1/32 microsteps. The LS7290 uses 32 microstepping phase controls for each motor step in half step or in 1/4, 1/8, 1/16 or 1/32 microsteps. The LS7290 uses stepping as shown in Table 2 for full step control. A table pointer is used which is incremented or decremented by a value determined by the operating mode and the direction control. The 8-bit PWM control and the refresh rate are set using an internal oscillator controlled by a crystal or by use of an external input clock. Typical refresh rate is equal to 31.25kHz. The LS7290 also contains two comparators for disabling drive to each motor coil if an overcurrent condition exists. This is sensed using a fractional-Ohm resistor in each of the two motor coil drive circuits.

INPUT/OUTPUT DESCRIPTION

$\overline{\text{RESET}}$ Input
Active low. Resets the PWM table pointer to HOME position per Table 2 and brings $\overline{\text{INH1}}$ and $\overline{\text{INH2}}$ low. Upon power-up, a POR circuit also resets the PWM table pointer.

$\overline{\text{ENABLE}}$ Input
Active low. When high (inactive), brings PHA, PHB, PHC, PHD, $\overline{\text{INH1}}$ and $\overline{\text{INH2}}$ outputs low.

$\overline{\text{STEP}}$ Input
Active low.
A low-going pulse on this input causes the motor to advance one step.

FRD/$\overline{\text{RVRS}}$ Input
A low input causes the motor to move in decremental steps per Table 2.
A high input causes the motor to move in incremental steps per Table 2
Switching directions can occur at any time.

PIN ASSIGNMENT
TOP VIEW

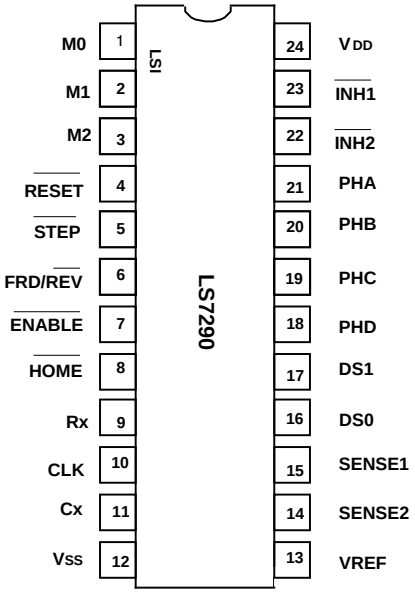


FIGURE 1

M0, M1, M2 Inputs
Defines the stepping modes as follows:

	M2	M1	M0
full step mode	0	0	0
1/2 step mode	0	0	1
1/4 step mode	0	1	0
1/8 step mode	0	1	1
1/16 step mode	1	0	0
1/32 step mode	1	0	1
1/32 step mode	1	1	0
1/32 step mode	1	1	1

Stepping Mode can be changed at any time.

SENSE1 / SENSE2 Inputs
The voltage on these comparator inputs are compared to an external reference to sense if an overcurrent condition exists. If a peak current causes the voltage across the external sense resistor to exceed the reference voltage, a latch is set and the drivers associated with the corresponding comparator are cut off. The next clock pulse samples the overcurrent condition and, if it no longer exists, resets the latch. Otherwise the latch remains set until the following clock pulse.

VREF Input
External voltage reference for overcurrent comparators.

Rx, Cx, CLK
These three pins can be configured in one of three ways to obtain the primary clock. A crystal connected between Rx and CLK pins or a resistor-capacitor pair connected among all three pins (see Figure 4) can make use of the internal oscillator. Alternatively, the CLK pin can be driven from an external clock source.

DS0 / DS1 Inputs
The phase drive is blanked out between steps by switching outputs $\overline{INH1}$ and $\overline{INH2}$ low in order to reduce audible noise and power consumption. The duration of the blanking is selected by DS0 and DS1 according to Table 1

Table 1

DS1	DS0	Blanking Time, IPB, at fc = 8MHz
0	0	1.25us
0	1	2.50us
1	0	3.75us
1	1	5.00us

PHA / PHB / PHC / PHD Outputs
The state of these phase outputs are determined by the look-up table and are used to control either the left or right half of each of the H-Bridge drivers. A low on a phase output enables the bottom driver while a high on the output enables the top driver.

$\overline{HOME}$ Output
Indicates Step0 state per Table 2 with a logic low.

$\overline{INH1}$ / $\overline{INH2}$ Outputs
These outputs are used to provide PWM control to each of the two H-Bridge drivers.

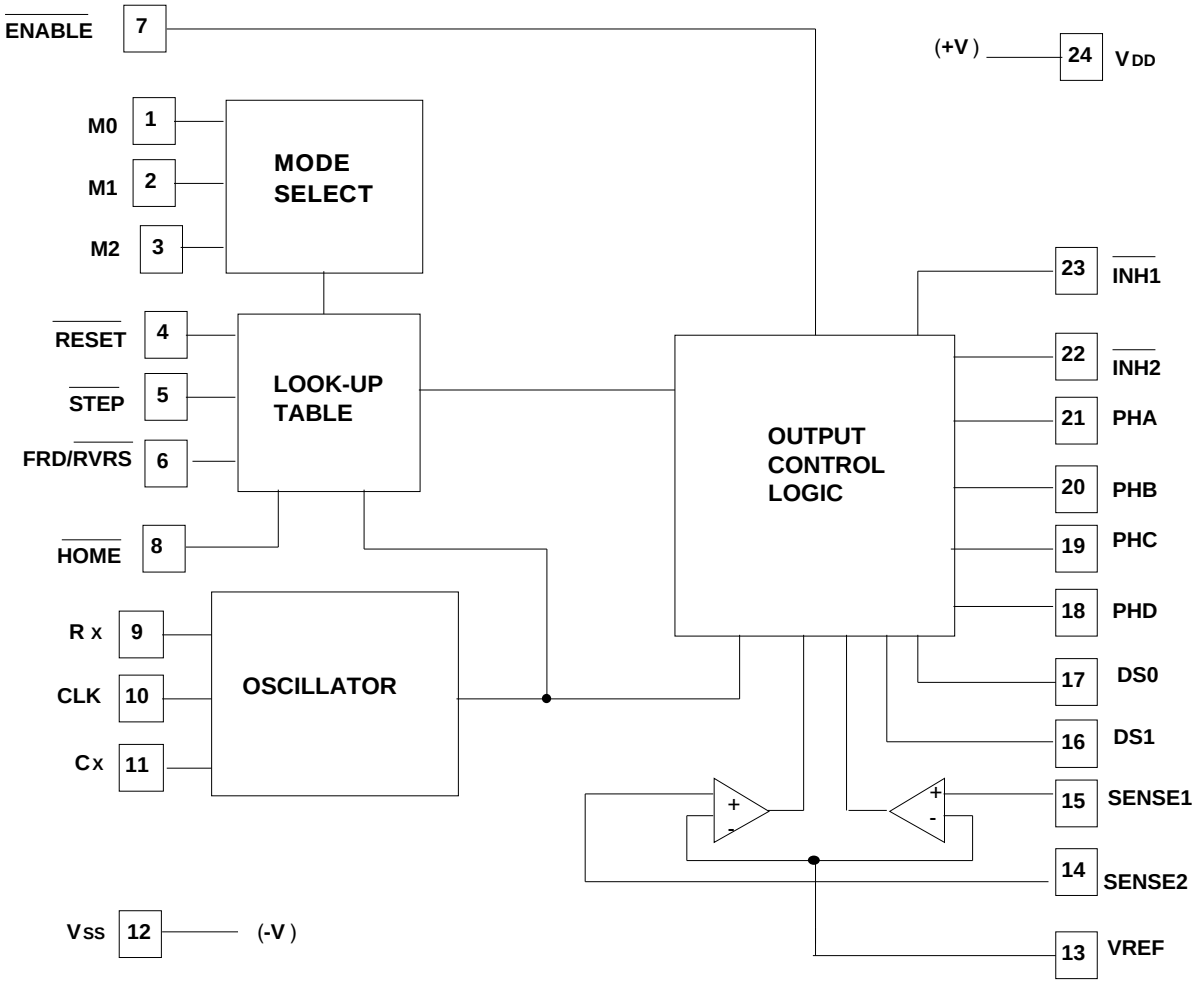
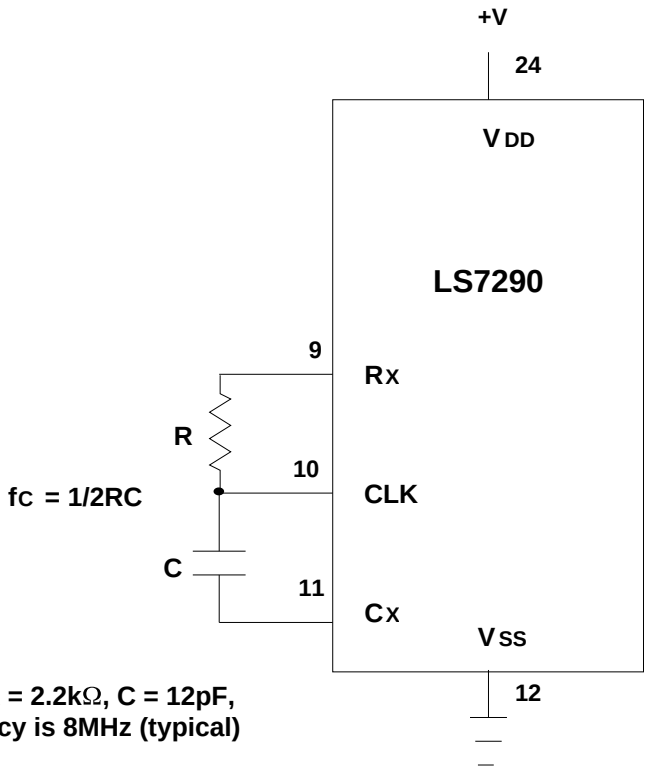


FIGURE 2. LS7290 BLOCK DIAGRAM

ELECTRICAL SPECIFICATIONS (-25°C < T_A < +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	CONDITIONS
Supply Voltage	V_{DD}	3.0	-	5.5	V	-
Supply Current	I_{DD}		-	2.0	mA	Outputs floating, Inputs high
CLK frequency	f_c	-	8.00	-	MHz	-
Enable Propagation Delay	t_{epd}	100	-	-	ns	-
FRD / RVRS Setup Time (before step pulse)	t_{ds}	0	-	-	us	-
Step Pulse Width	SPW	1.0	-	-	us	at f_c = 8 MHz
Interstep Pulse Delay	ISD	32	-	-	us	at f_c = 8 MHz
Interstep Phase Blanking	IPB	1.25	-	5.0	us	at f_c = 8 MHz
Reset Pulse Width	RPW	1.0	-	-	us	at f_c = 8 MHz
Reset to Step Pulse Delay	t_{rs}	0	-	-	us	-
Hi-Level Input Voltage	V_{iH}	2	-	-	V	V_{DD} = 5 ± 0.25V
Low-Level Input Voltage	V_{IL}	-	-	0.8	V	V_{DD} = 5 ± 0.25V
Hi-Level Input Current	I_H	-	-	50	nA	Leakage Current
Low-Level Input Current	I_L	-	-	50	nA	Leakage Current
Output Sink Current	Io	-10	-	-	mA	Vo = 0.4V, V_{DD} = 5V
	Io	-5	-	-	mA	Vo = 0.4V, V_{DD} = 3.3V
Output Source Current	Io	5	-	-	mA	Vo = 4.0V, V_{DD} = 5V
	Io	2.5	-	-	mA	Vo = 2.5V, V_{DD} = 3.3V
Comparator Offset Voltage	V_{OS}	-	5	15	mV	V_{REF} = 1V
Input Reference Voltage	V_{REF}	0.5	-	3.0	V	V_{DD} = 5V
	V_{REF}	0.5	-	1.5	V	V_{DD} = 3.3V



At V_{DD} = 5V and R = 2.2kΩ, C = 12pF, oscillator frequency is 8MHz (typical)

FIGURE 3. RC OSCILLATOR FOR CLOCK GENERATOR

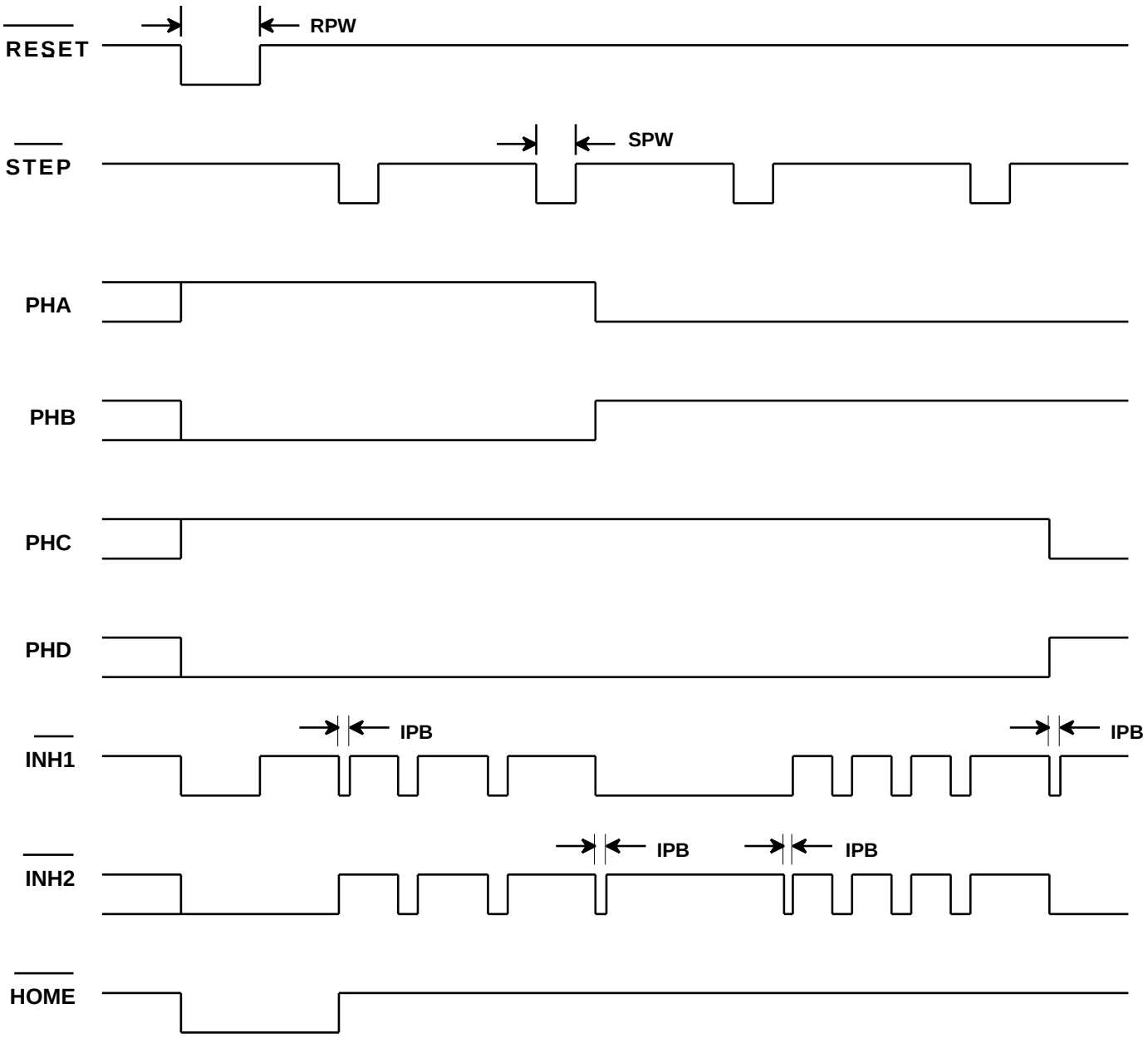


FIGURE 4. PARTIAL SEQUENCE IN FORWARD 1/2 STEP MODE

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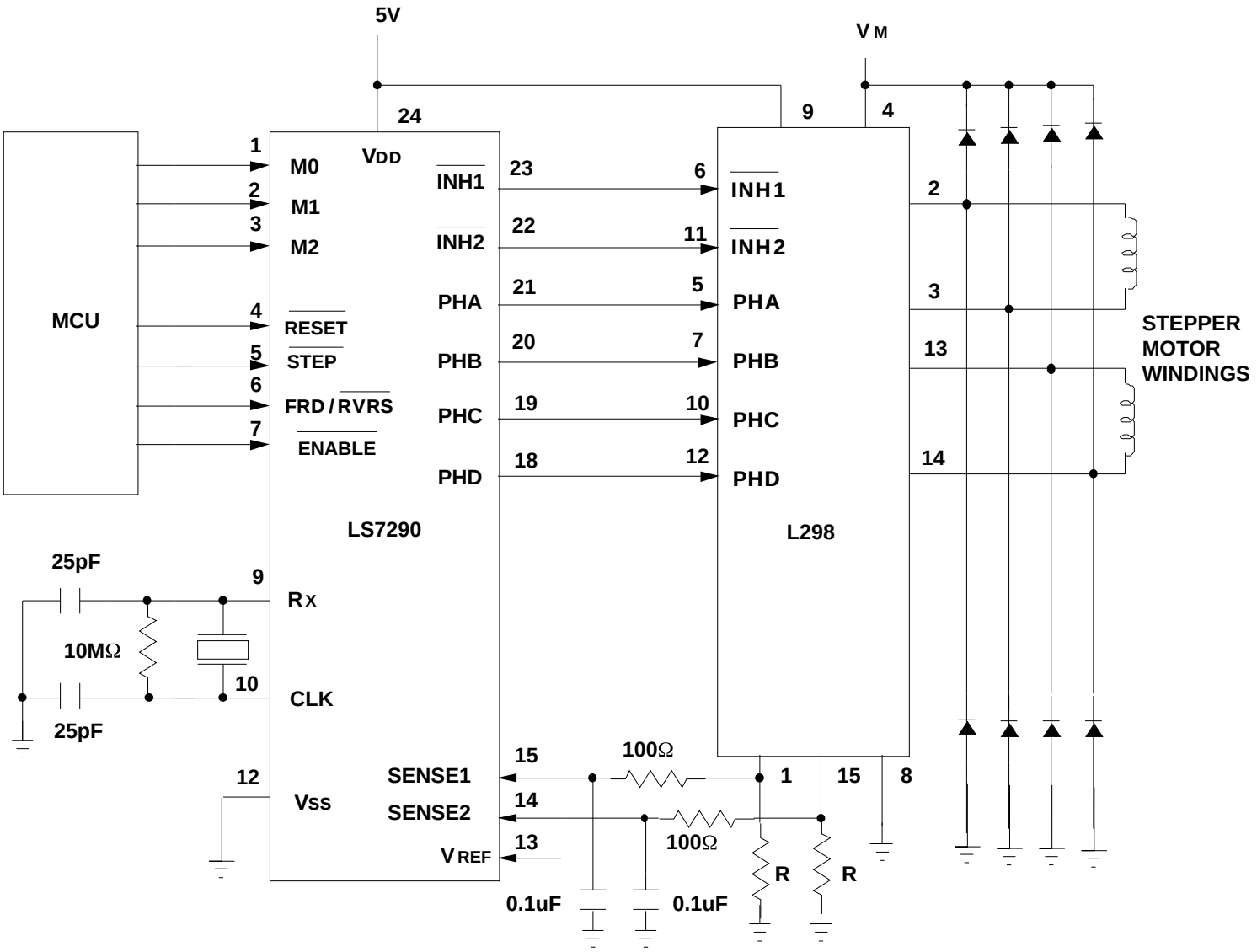

FIGURE 5. TYPICAL APPLICATION SCHEMATIC FOR A TWO-PHASE BIPOLAR MOTOR USING A SINGLE MOTOR DRIVER IC

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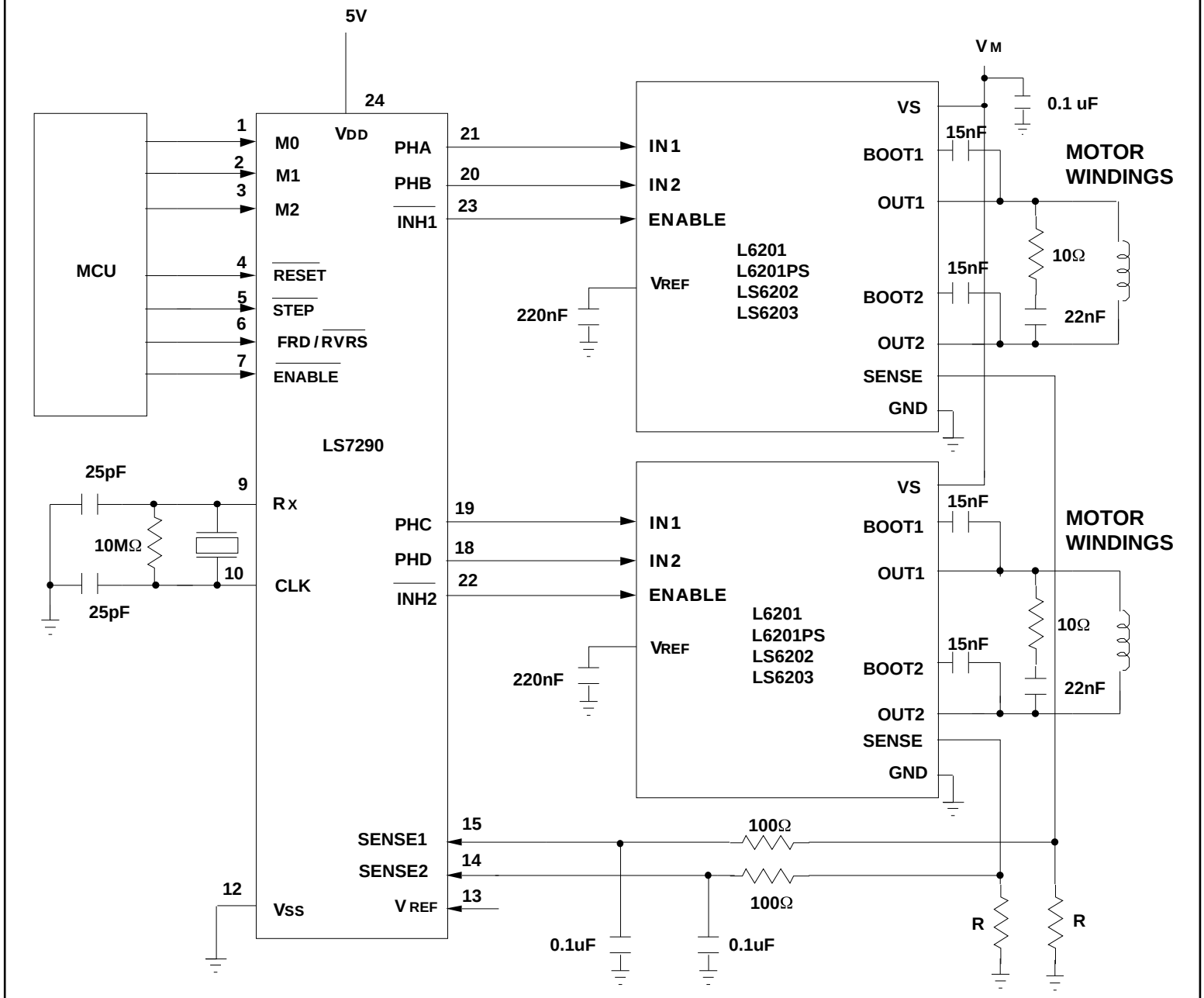

FIGURE 6. TYPICAL APPLICATION SCHEMATIC FOR A TWO-PHASE BIPOLAR MOTOR USING TWO SEPARATE MOTOR DRIVER ICs

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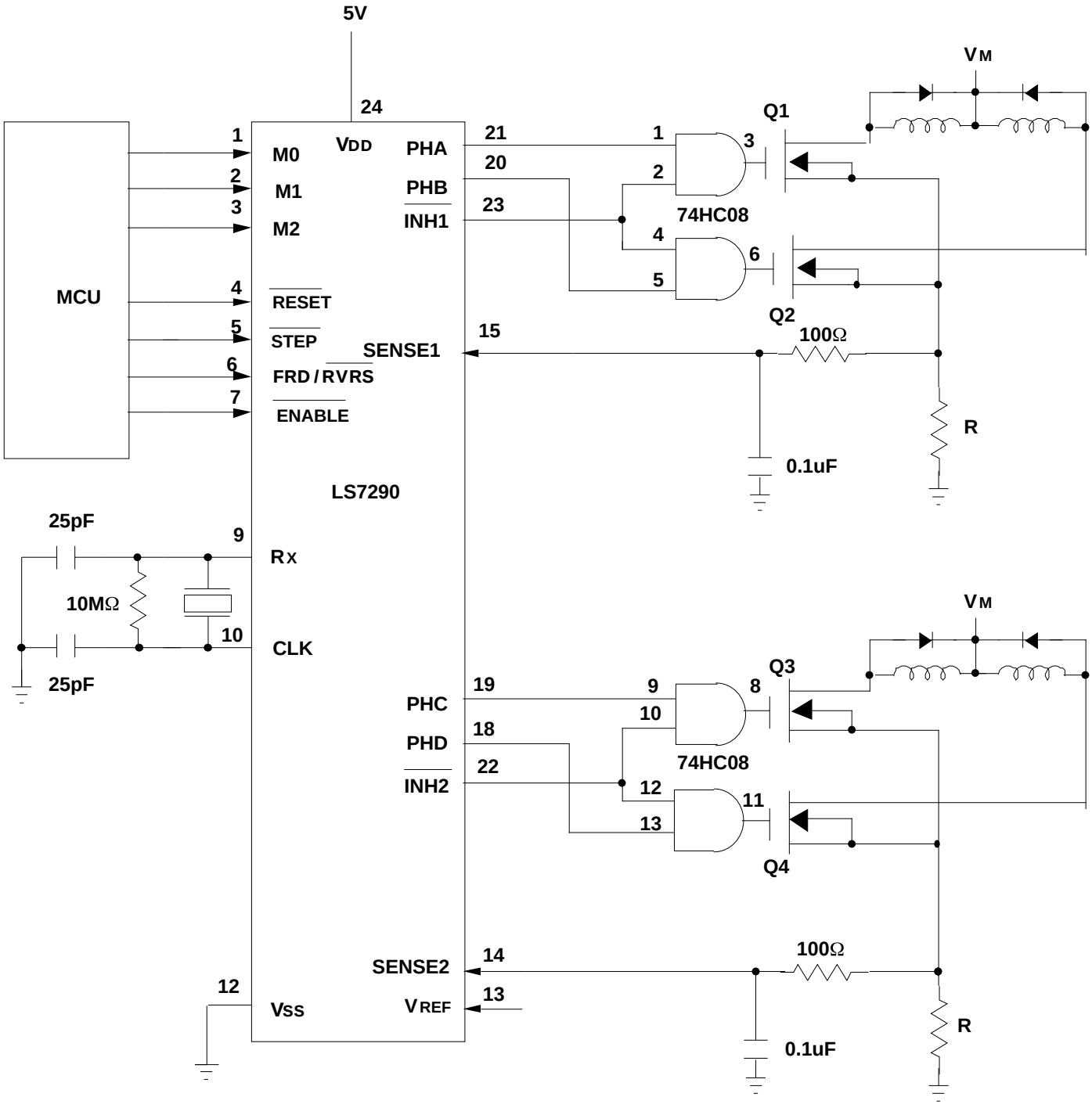

NOTE: Q1, Q2, Q3, Q4 are MOSFET Power Transistors suitable for 5V Gate Drive
Typical P/Ns = IRLZ44N and IRF3708

FIGURE 7. TYPICAL APPLICATION SCHEMATIC FOR A FOUR-PHASE UNIPOLAR MOTOR USING DISCRETE MOSFET TRANSISTORS

TABLE 2

Step Number						% Duty Cycle		Phases				
Full	1/2	1/4	1/8	1/16	1/32	$\overline{INH1}$	$\overline{INH2}$	PHA	PHB	PHC	PHD	Step Angle
0	0	0	0	0	0	100.0	0.0	1	0	1	0	HOME
					1	99.9	4.9	1	0	1	0	2.81
				1	2	99.5	9.8	1	0	1	0	5.63
					3	98.9	14.7	1	0	1	0	8.44
			1	2	4	98.1	19.5	1	0	1	0	11.25
					5	97.0	24.3	1	0	1	0	14.06
				3	6	95.7	29.0	1	0	1	0	16.88
					7	94.2	33.7	1	0	1	0	19.69
		1	2	4	8	92.4	38.3	1	0	1	0	22.50
					9	90.4	42.8	1	0	1	0	25.31
				5	10	88.2	47.1	1	0	1	0	28.13
					11	85.8	51.4	1	0	1	0	30.94
			3	6	12	83.1	55.6	1	0	1	0	33.75
					13	80.3	59.6	1	0	1	0	36.56
				7	14	77.3	63.4	1	0	1	0	39.38
					15	74.1	67.2	1	0	1	0	42.19
	1	2	4	8	16	70.7	70.7	1	0	1	0	45.00
					17	67.2	74.1	1	0	1	0	47.81
				9	18	63.4	77.3	1	0	1	0	50.63
					19	59.6	80.3	1	0	1	0	53.44
			5	10	20	55.6	83.1	1	0	1	0	56.25
					21	51.4	85.8	1	0	1	0	59.06
				11	22	47.1	88.2	1	0	1	0	61.88
					23	42.8	90.4	1	0	1	0	64.69
		3	6	12	24	38.3	92.4	1	0	1	0	67.50
					25	33.7	94.2	1	0	1	0	70.31
				13	26	29.0	95.7	1	0	1	0	73.13
					27	24.3	97.0	1	0	1	0	75.94
			7	14	28	19.5	98.1	1	0	1	0	78.75
					29	14.7	98.9	1	0	1	0	81.56
				15	30	9.8	99.5	1	0	1	0	84.38
					31	4.9	99.9	1	0	1	0	87.19
1	2	4	8	16	32	0.0	100.0	0	1	1	0	90.00
					33	-4.9	99.9	0	1	1	0	92.81
				17	34	-9.8	99.5	0	1	1	0	95.63
					35	-14.7	98.9	0	1	1	0	98.44
			9	18	36	-19.5	98.1	0	1	1	0	101.25
					37	-24.3	97.0	0	1	1	0	104.06
				19	38	-29.0	95.7	0	1	1	0	106.88

TABLE 2 (continued)

Step Number						% Duty Cycle		Phases				
Full	1/2	1/4	1/8	1/16	1/32	$\overline{INH1}$	$\overline{INH2}$	PHA	PHB	PHC	PHD	Step Angle
					39	-33.7	94.2	0	1	1	0	109.69
		5	10	20	40	-38.3	92.4	0	1	1	0	112.50
					41	-42.8	90.4	0	1	1	0	115.31
				21	42	-47.1	88.2	0	1	1	0	118.13
					43	-51.4	85.8	0	1	1	0	120.94
			11	22	44	-55.6	83.1	0	1	1	0	123.75
					45	-59.6	80.3	0	1	1	0	126.56
				23	46	-63.4	77.3	0	1	1	0	129.38
					47	-67.2	74.1	0	1	1	0	132.19
	3	6	12	24	48	-70.7	70.7	0	1	1	0	135.00
					49	-74.1	67.2	0	1	1	0	137.81
				25	50	-77.3	63.4	0	1	1	0	140.63
					51	-80.3	59.6	0	1	1	0	143.44
			13	26	52	-83.1	55.6	0	1	1	0	146.25
					53	-85.8	51.4	0	1	1	0	149.06
				27	54	-88.2	47.1	0	1	1	0	151.88
					55	-90.4	42.8	0	1	1	0	154.69
		7	14	28	56	-92.4	38.3	0	1	1	0	157.50
					57	-94.2	33.7	0	1	1	0	160.31
				29	58	-95.7	29.0	0	1	1	0	163.13
					59	-97.0	24.3	0	1	1	0	165.94
			15	30	60	-98.1	19.5	0	1	1	0	168.75
					61	-98.9	14.7	0	1	1	0	171.56
				31	62	-99.5	9.8	0	1	1	0	174.38
					63	-99.9	4.9	0	1	1	0	177.19
2	4	8	16	32	64	-100.0	0.0	0	1	0	1	180.00
					65	-99.9	-4.9	0	1	0	1	182.81
				33	66	-99.5	-9.8	0	1	0	1	185.63
					67	-98.9	-14.7	0	1	0	1	188.44
			17	34	68	-98.1	-19.5	0	1	0	1	191.25
					69	-97.0	-24.3	0	1	0	1	194.06
				35	70	-95.7	-29.0	0	1	0	1	196.88
					71	-94.2	-33.7	0	1	0	1	199.69
		9	18	36	72	-92.4	-38.3	0	1	0	1	202.50
					73	-90.4	-42.8	0	1	0	1	205.31
				37	74	-88.2	-47.1	0	1	0	1	208.13
					75	-85.8	-51.4	0	1	0	1	210.94
			19	38	76	-83.1	-55.6	0	1	0	1	213.75
					77	-80.3	-59.6	0	1	0	1	216.56
				39	78	-77.3	-63.4	0	1	0	1	219.38
					79	-74.1	-67.2	0	1	0	1	222.19
	5	10	20	40	80	-70.7	-70.7	0	1	0	1	225.00
					81	-67.2	-74.1	0	1	0	1	227.81
				41	82	-63.4	-77.3	0	1	0	1	230.63
					83	-59.6	-80.3	0	1	0	1	233.44

TABLE 2 (continued)

Step Number						% Duty Cycle		Phases				
Full	1/2	1/4	1/8	1/16	1/32	$\overline{INH1}$	$\overline{INH2}$	PHA	PHB	PHC	PHD	Step Angle
			21	42	84	-55.6	-83.1	0	1	0	1	236.25
					85	-51.4	-85.8	0	1	0	1	239.06
				43	86	-47.1	-88.2	0	1	0	1	241.88
					87	-42.8	-90.4	0	1	0	1	244.69
		11	22	44	88	-38.3	-92.4	0	1	0	1	247.50
					89	-33.7	-94.2	0	1	0	1	250.31
				45	90	-29.0	-95.7	0	1	0	1	253.13
					91	-24.3	-97.0	0	1	0	1	255.94
			23	46	92	-19.5	-98.1	0	1	0	1	258.75
					93	-14.7	-98.9	0	1	0	1	261.56
				47	94	-9.8	-99.5	0	1	0	1	264.38
					95	-4.9	-99.9	0	1	0	1	267.19
3	6	12	24	48	96	0.0	-100	1	0	0	1	270.00
					97	4.9	-99.9	1	0	0	1	272.81
				49	98	9.8	-99.5	1	0	0	1	275.63
					99	14.7	-98.9	1	0	0	1	278.44
			25	50	100	19.5	-98.1	1	0	0	1	281.25
					101	24.3	-97.0	1	0	0	1	284.06
				51	102	29.0	-95.7	1	0	0	1	286.88
					103	33.7	-94.2	1	0	0	1	289.69
		13	26	52	104	38.3	-92.4	1	0	0	1	292.50
					105	42.8	-90.4	1	0	0	1	295.31
				53	106	47.1	-88.2	1	0	0	1	298.13
					107	51.4	-85.8	1	0	0	1	300.94
			27	54	108	55.6	-83.1	1	0	0	1	303.75
					109	59.6	-80.3	1	0	0	1	306.56
				55	110	63.4	-77.3	1	0	0	1	309.38
					111	67.2	-74.1	1	0	0	1	312.19
	7	14	28	56	112	70.7	-70.7	1	0	0	1	315.00
					113	74.1	-67.2	1	0	0	1	317.81
				57	114	77.3	-63.4	1	0	0	1	320.63
					115	80.3	-59.6	1	0	0	1	323.44
			29	58	116	83.1	-55.6	1	0	0	1	326.25
					117	85.8	-51.4	1	0	0	1	329.06
				59	118	88.2	-47.1	1	0	0	1	331.88
					119	90.4	-42.8	1	0	0	1	334.69
		15	30	60	120	92.4	-38.3	1	0	0	1	337.50
					121	94.2	-33.7	1	0	0	1	340.31
				61	122	95.7	-29.0	1	0	0	1	343.13
					123	97.0	-24.3	1	0	0	1	345.95
			31	62	124	98.1	-19.5	1	0	0	1	348.75
					125	98.9	-14.7	1	0	0	1	351.56
				63	126	99.5	-9.8	1	0	0	1	354.38
					127	99.9	-4.9	1	0	0	1	357.19
0	0	0	0	0	0	100.0	0.0	1	0	1	0	HOME